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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/000,440	10/30/2001	Gerald H. Johnson	1495-US	9174

7590 06/11/2003

Legal Department
Teradyne, Inc.
321 Harrison Avenue
Boston, MA 02118

EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/000,440	JOHNSON, GERALD H.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is indefinite because it is unclear as to how the control path (static control path) can be "static" since it receiving a feedback signal from the output (the output of the path will be varied when the output put signal varies).

Claims 2-7 are rejected as including the indefiniteness of claim 1.

Claim 8 is indefinite because it is unclear as to how the error signal would be static since if varies responsive to the output signal (further see the rejection of claim 1).

Claim 9 is indefinite as including the indefiniteness of claim 8.

Claim 10 is indefinite because it is unclear as to how the control path (static control path) can be "static" since it receiving a feedback signal from the output (the output of the path will be varied when the output put signal varies).

Claims 11-16 are rejected as including the indefiniteness of claim 10.

Claim 17 is indefinite because it is unclear as to how the error signal would be static since if varies responsive to the output signal (further see the rejection of claim 1).

Claims 18 and 19 are as including the indefiniteness of claim 17.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 4, 5, 10, 13, 14, 17 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Takenaka (USP 5504452).

As to claim 1, Takenada discloses in figure 2 control loop circuit for optimizing a power supply output under varying load conditions (the limitation "under varying load conditions" is seen as intended use limitation, and Takenaka figure 2 is capable of providing supply voltage under varying load condition), the power supply having a main loop amplifier (12) and an output stage (24, 26) (column 4, lines 48, defines VNN as "an output voltage") to generate the output, the control loop circuit including: a static control path (23, 24, 26) coupled to the output (VNN) and having an error amplifier (23), the error amplifier operative to generate an error signal (COMP) for presentation to the main loop amplifier, the error signal representing the difference between a desired output (Vref) and a sensed output (the path comprising circuit 23 performs similar functions as claimed, therefore the path is seen as "static" path) ; and a dynamic control path (15, 16) coupled to the error amplifier output and responsive to the error signal to generate a dynamic compensation signal, the dynamic control path having an output coupled to the main loop amplifier output.

As to claim 4, figure 2 the dynamic control path is disposed in parallel with the static control path.

As to claim 5, figure 2 shows the dynamic control path is selectively activated when the error signal is greater than a predetermined threshold (transistor 32 is active when the COMP signal is greater than the threshold of the p-channel transistor in inverter 33).

As to claim 10, figure 2 shows a power supply system including: a main loop amplifier (12) circuit; an output stage (24, 26) (column 4, lines 48) disposed in cascade with the main loop amplifier circuit; and a control loop circuit, the control loop circuit including a static control path (23, 24, 26) coupled to the output (VNN) and having an error amplifier (23), the error amplifier operative to generate an error signal for presentation to the main loop amplifier, the error signal representing the difference between a desired output (Vref) and a sensed output; and a dynamic control path (16) coupled to the error amplifier output and responsive to the error signal to generate a dynamic compensation signal, the dynamic control path having an output coupled to the main loop amplifier output.

As to claim 13, figure 2 shows the dynamic control path is disposed in parallel with the static control path.

As to claim 14, figure 2 shows the dynamic control path is selectively activated when the error signal is greater than a predetermined threshold (transistor 32 is active when the COMP signal is greater than the threshold of the p-channel transistor in inverter 33).

As to claim 17, figure 2 shows a method of controlling the output of a DUT power supply (the limitation DUT is seen as intended use, circuit figure 2 is capable of providing power supply to DUT), the method including the steps of: generating a static error signal (output of 12) based on the difference between the desired power supply (Vref) output and the actual power supply

output (VNN); producing a dynamic error signal (output of 15) in parallel with the static error signal; and summing the static error signal and dynamic error signal to create an optimal compensation signal.

As to claim 18, figure 2 shows the producing step is dependent on the magnitude of the static error signal being above a pre-set threshold (the threshold of the p-channel transistor in 33).

Allowable Subject Matter

5. Claims 2, 3, 6, 7, 11, 12, 15, 16 and 19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims and if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 8 and 9 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Claims 2, 3, 6, 7, 11, 15, 16 and 19 would be allowable because the prior art fails to teach or suggest a circuit, and method thereof, (such as figure 2) having a dynamic control path (72), the dynamic control path includes: input conversion circuitry (ADC1) for converting the error signal (output of 32) into a digital signal, a digital-signal-processor (DSP) coupled to the conversion circuitry; a look-up table (memory) for storing optimal compensation signal responses to detected error signals, the DSP operative in response to the digitized error signal to access the look-up table and identify the optimal compensation signal, and generating the optimal signal; and output conversion circuitry (DAC2, DAC3) for feeding the optimal signal to the main loop amplifier output.

Claims 8 and 9 would be allowable because the limitation "means for statically generating an error signal' is the means plus function limitation. Clearly, Takenaka's error amplifier circuit (23) does not have similar structure, nor have equivalent function with Applicant's error amplifier circuit (35 U.S.C. 112, sixth paragraph and MPEP § 2181 through § 2186).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
June 9, 2003

Quan Tra
Art Unit 2816